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Implementation of ALU for Reconfigurable Logic

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Abstract

In this work we have implemented an arithmetic and logic unit for reconfigurable logic. Arithmetic and logic unit proposed in this design supports 8 operations including 4 arithmetic and 4 logic operations. Further we have proposed one more ALU supporting 15 instructions with the inclusion of BCD operations and rotate and shift operations. The target device is KINTEX 7, 28nm technology.

Keywords: *dynamic power consumption, FPGA, arithmetic and logic unit, reconfigurable logic.*

1. Introduction

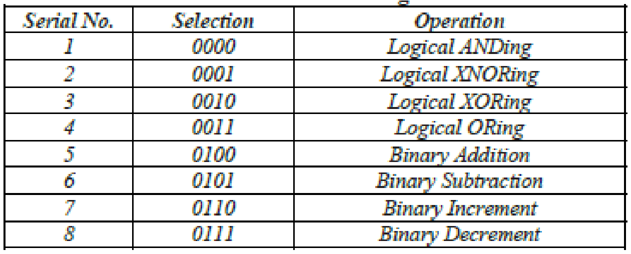
This is an era of hand held devices and equipments, most of these devices runs on battery, this puts a constraint on standby time, to increase standby time more and more battery life is needed, one way of solving this issue is to reduce power consumption of device or equipment. These days almost every device is intelligent, this intelligence came from using processors, and in forthcoming years this trend is likely to be increase. But these processors consume lot of the power of device as lot of switching activity is going inside. ALU (Arithmetic and Logic Unit) is the heart of any processor; this also consumes most of the processor power.

2. Conventional Eight Operation Design

The operations supported by proposed design are listed in table 1 and the block diagram of reference design is shown in figure 1. As shown in table 1 that the proposed design can perform 8 logical and arithmetic and logical operations. Eight units are used to implement the eight operations. At any given time instant only one of the eight units will be in use to perform one of the eight operations but clock signal CLK is assigned to all the eight units at all times, this increases the dynamic power consumption of the design.

Figure 2 shows the internal structure of logical AND operation. The AND operation is implemented by an array of AND gates followed by a D flip flop.

Table 1 Operations Supported by 8 Operations Conventional Design



Serial No.	*Selection*	*Operation*
1	*0000*	*Logical ANDing*
2	*0001*	*Logical XNORing*
3	*0010*	*Logical XORing*
4	*0011*	*Logical ORing*
5	*0100*	*Binary Addition*
6	*0101*	*Binary Subtraction*
7	*0110*	*Binary Increment*
8	*0111*	*Binary Decrement*

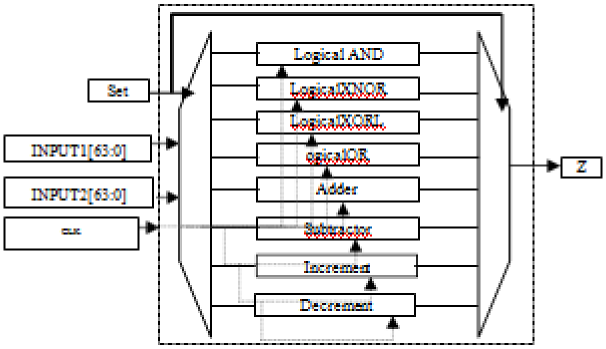


Fig. 1 Conventional 8 Operation Design - Internal Architecture

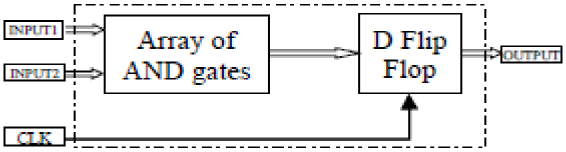


Fig 2: Internal Structure - Logical AND

Similarly internal structures of all the units are shown in figure 2 to figure 9.

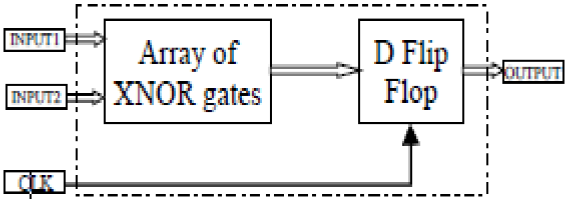


Fig 3: Internal Structure - Logical XNOR

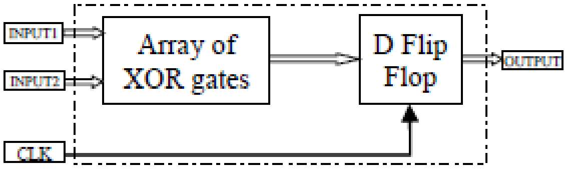


Fig 4: Internal Structure - Logical XOR

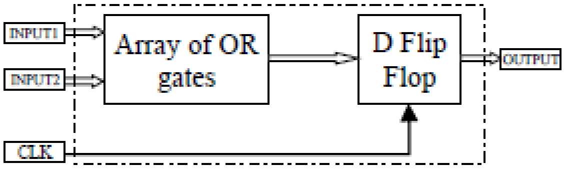


Fig 5: Internal Structure - Logical OR

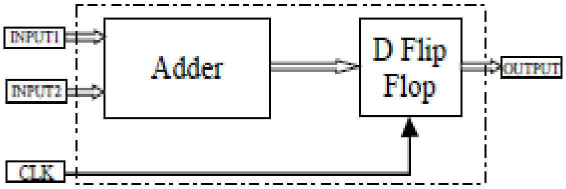


Fig 6: Internal Structure - Adder

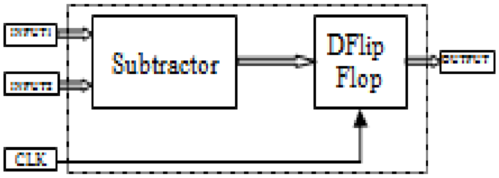


Fig 7: Internal Structure - Subtractor

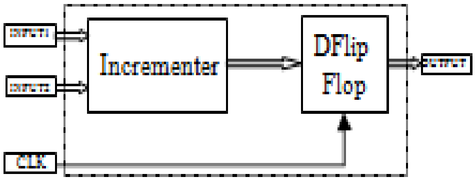


Fig 8: Internal Structure - Incrementer

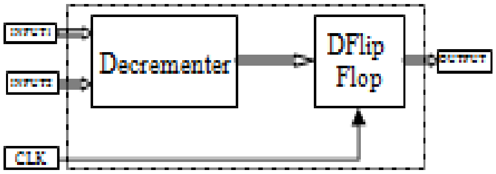


Fig 9: Internal Structure -Decrementer

3. Conventional Fifteen Operation Design

This section discusses the conventional ALU supporting fifteen operations, this ALU is based on the same design as the reference ALU supporting eight operations i.e. clock is available to all the units at all time and different units are used for performing addition, subtraction, increment and decrement. Here in this design we have incorporated 7 more instructions to perform shift, rotate and BCD operations. Table 2 shows the supported operations by this design.

Table 2 Reference ALU – 15 Instructions

Serial No.	*Selection*	*Operation*
1	*0000*	*Logical ANDing*
2	*0001*	*Logical XNORing*
3	*0010*	*Logical XORing*
4	*0011*	*Logical ORing*
5	*0100*	*Binary Addition*
6	*0101*	*Binary Subtraction*
7	*0110*	*Binary Increment*
8	*0111*	*Binary Decrement*
9	*1000*	*Rotate Right*
10	*1001*	*Rotate Left*
11	*1010*	*Shift Right*
12	*1011*	*Shift Left*
13	*1100*	*BCD Addition*
14	*1101*	*BCD Subtraction*
15	*1110*	*BCD Multiplication*
16	*1111*	*NOP*

Figure 110 shows the internal architecture of reference ALU –15 operations, no clock gating logic is used and separate blocks are used to perform addition, subtraction, increment and decrement.

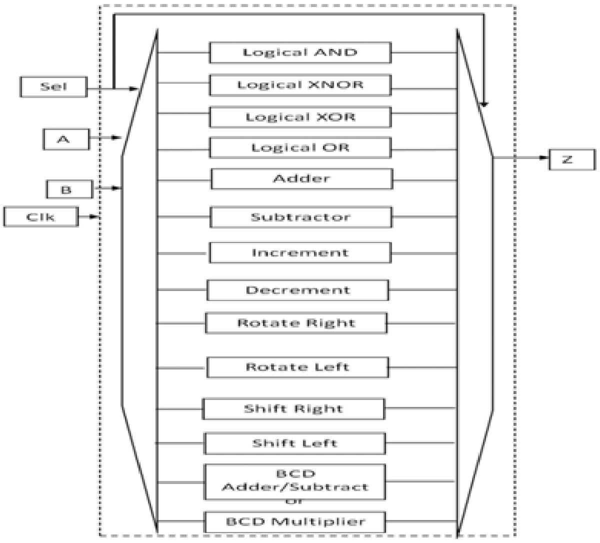


Fig. 10 Conventional 15 operation ALU – Internal Architecture

The rotate right operation is shown in figure 11, it consists of connections with input and out ports and 64 D flip flops (FD) as shown in figure. The first input signal I0 is connected to output signal O63, I1 to O0, I2 to O1 and so on. Similarly architectures of rotate and shift operations are shown in figure 12 – 14.

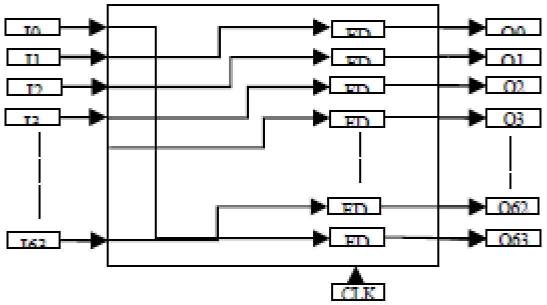


Fig. 11 Rotate Right – Internal Structure

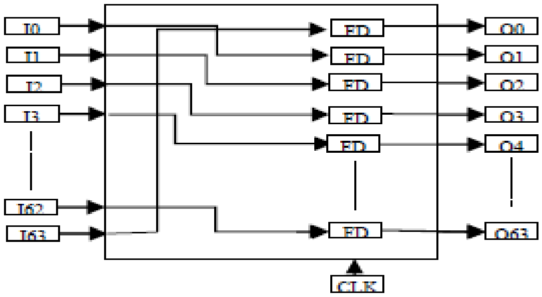


Fig. 12 Rotate Left – Internal Structure

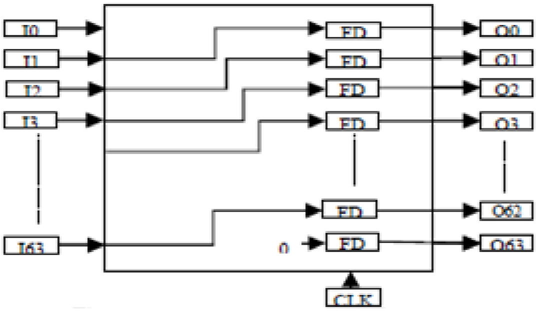


Fig.13 Shift Left – Internal Structure

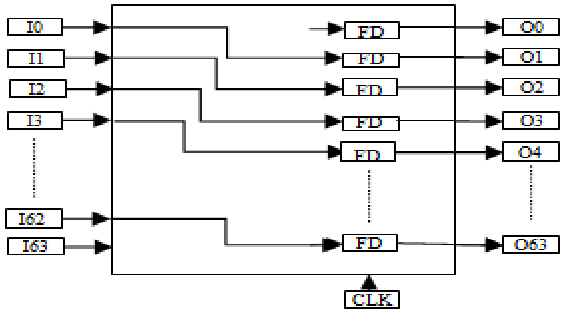


Fig.14 Shift Right – Internal Structure

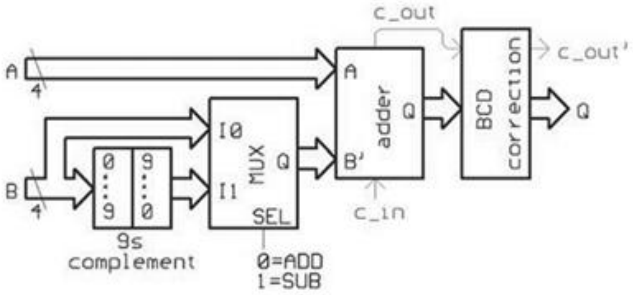


Fig.15 BCD Adder/Subtractor

The BCD adder/Subtractor unit shown in figure 15 consists of a binary adder with a BCD correction unit to perform the addition, to perform the subtraction also a 9'complement unit is also incorporated shown in figure 18. Here in figure 15 a multiplexer is also incorporated to select between the BCD addition and BCD subtraction. To perform BCD addition the data path is the simply the multiplexer, then the binary adder and then the BCD correction unit. To perform the subtraction. first the 9's complement of the second number is calculated using the 9'complement unit and the multiplexer passes this complemented number to the binary adder to perform the subtraction, the final result of BCD subtraction is obtained after the BCD correction has been performed.

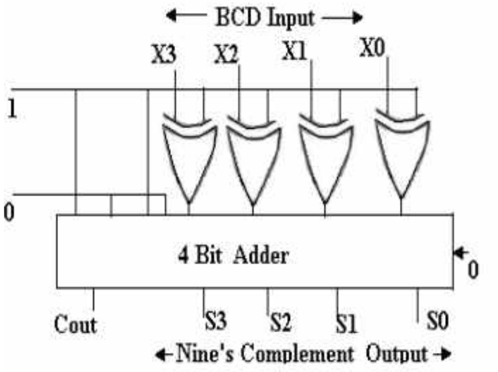


Fig.16 9's Complement Unit

The 9's complement is performed using 4 xor gates, which XORes the input number with 1 and a binary adder to perform the addition of 0110 with the xored number. Figure 17 represents an area optimized BCD digit multiplier. This multiplier produces the result of multiplication in binary and we need a binary to BCD converter shown in figure 18. The B is the higher nibble of the multiplication and C is the lower nibble of multiplication. Figure 19 shows the parallel multiplication process of a 4 x 4 BCD multiplier. Xi and yi are single digit BCD numbers. These numbers are multiplied using the single digit BCD multiplier shown in figures. pyixiH and pyixiL are higher and lower nibble of multiplication respectively. Figure 20 depicts the 4 x 4 multiplier architecture to implement the algorithm shown figure. In the process of floating point multiplication this 4x4 multiplier is extended to implement 16 x 16 multiplier.

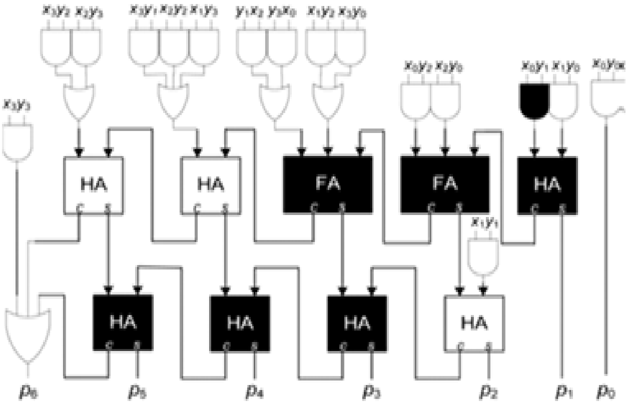


Fig.17 Area optimized – Single digit BCD Multiplier

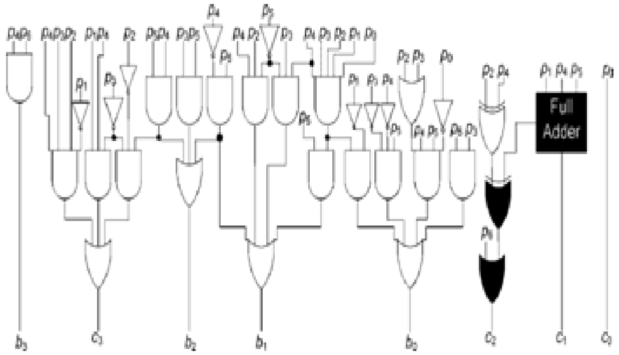


Fig.18 Binary to BCD Converter

				x3	x2	x1	x0
				y3	y2	y1	y0
				P0003L	P0002L	P0001L	p0000L
			P0003H	P0002H	P0001H	P0000H	
			P0103L	P0102L	P0101L	P0100L	
		P0103H	P0102H	P0101H	P0100H		
		P0203L	P0202L	P0201L	P0200L		
	P0203H	P0202H	P0201H	P0200H			
	P0303L	P0302L	P0301L	P0300L			
P0303H	P0302H	P0301H	P0300H				
P7	P6	P5	P4	P3	P2	P1	P0

Fig.19 Array BCD Multiplication Process

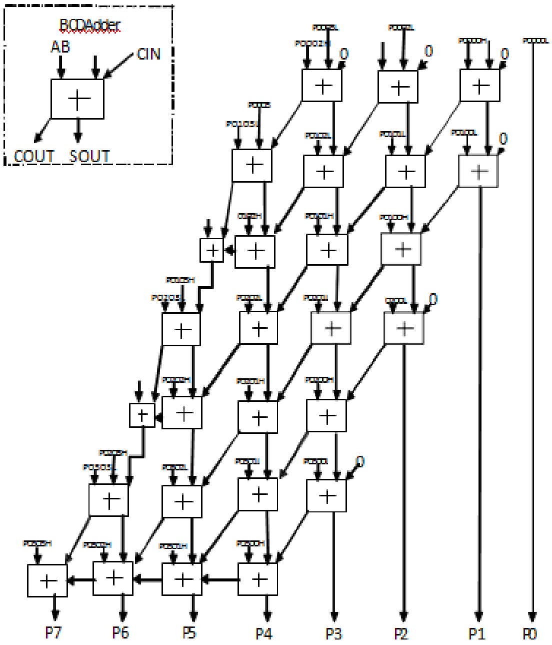


Fig.20 4 digit BCD Multiplier

4. Performance Analysis

Table 3 shows the resource and power consumption of reference ALU and area and power efficient ALU. The base paper design and the conventional design are same, we have implemented the base paper design [1] and named it conventional design.

Table 3 Performance analysis – 8 Operation designs

On Chip	Base Paper Design		Conventional	
	Power (mW)	Resource	Power (mW)	Resource
Clock	0.16	-	02	-
Logic	0.76	496	02	511
Signal	6.63	752	04	764
IOS	35.98	197	37	196
Static Power	45.32	-	45	-
Dynamic Power	43.53	-	44	-
Total	88.85	-	90	-

Table 4 shows the resource and power consumption of conventional ALU. The base paper design and the conventional design are same, we have implemented the base paper design and named it conventional design.

5. Conclusion

In this work we have successfully implemented an arithmetic and logic unit for reconfigurable logic. In this work two designs are implemented, first design is the conventional ALU supporting 8 operations. The second design is conventional design supporting 15 instructions, in this design we have increased the functionality of the base paper design by employing 7 more instructions making the design to support a total of 15 operations. The new 7 operations employs rotate right, rotate left, shift right, shift left, BCD addition, BCD subtraction and BCD multiplication.

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