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A REVIEW OF IMPLEMENTATION OF QUANTUM COMPUTING 4 BIT REVERSIBLE COMPARATOR

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ABSTRACT:

In these paper reversible logic circuits has attracted considerable attention in improving some fields like nanotechnology, quantum computing, and low power design. In this paper 4 bit reversible comparator based on classical logic circuit is represented which uses existing reversible gates. In this design we try to reduce optimization parameters like number of constant inputs, garbage outputs, and quantum cost. The results show that, the proposed comparator has 4 quantum cost and one constant input less than the prior design.

Keywords: *reversible gates; reversible comparator; quantum cost; constant inputs; garbage outputs.*

INTRODUCTION

Reversible logic has been considered as one of the promising practical strategies for power-efficient computing [1]. R. Landauer shows when one bit of information loses, KTln2 joules of energy dissipate (K is the Boltzman's constant and T is the operational temperature) [2]. Later, Bennett [3] proved that this energy could be saved by using reversible logic circuit. In fact, when the inputs cannot be recovered from circuit's outputs, information loss appears. Reversible logic circuits can handle this issue. In this logic, one to one mapping exists between the inputs and outputs, the number of inputs and outputs is equal, and inputs can be recovered from outputs. Reversible logic circuit utilizes in many applications such as nanotechnology, quantum computing, optical information processing, and quantum dot cellular automata (QCA). In order to achieving an optimized reversible circuit, some points should be considered: 1) Fan-out is forbidden. 2) Feedback and loop are not allowed. 3) Delay should be minimum. 4) Optimization parameters should be minimum. The parameters such as number of reversible gates, number of constant inputs, garbage outputs, and quantum cost (QC) can be named as optimization parameters and are defined as: 1) The inputs, which equal to 0 or 1, are constant inputs. 2) Garbage outputs are output vectors which do not generate any useful function. 3) Quantum cost refers to the cost of the circuit in terms of primitive gate [4].

In proposed paper, 4 bit reversible comparator is designed. First of all, some reversible logic gates, which are used in circuit construction, are described. Classical implementation of comparator is represented In this paper, 4 bit reversible comparator based on reversible logic gates is designed. Compared with prior designs, proposed circuit is optimized in number of constant inputs, number of garbage outputs and, quantum cost. This reversible circuit is useful for nanotechnology, quantum computing and low power design.

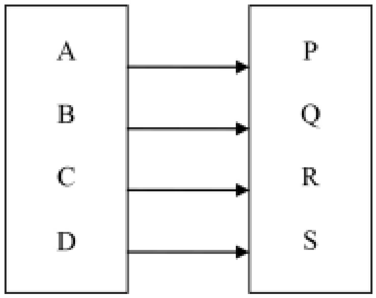

Fig. 1: Input and output mapping.

Research in reversible logic is getting importance today. Nagamani *et al.* presented reversible 1 bit comparatorsThe comparators were designed using BJN gate, Peres gate and Feynman gate. Lihui *et al.* proposedreversible 4 bit comparator using NLG gate NLG gate is a 2 × 2 reversible gate. The gate works on the principle that when both inputs are same second output is one. This is similar to EXNOR logic. It is considered as complement of Feynman gate. Haghparast *et al.* proposed a 4 bit comparator using subtraction logic usingHNG gate adopting carry propagation technique. It requires 4 HNG gates, 4 Peres gates and 2 Feynman gates for 4 bit comparator design. Molecular design of half subtractor using Tetraphenylporphyrin was discussedin Kaur *et al.* discussed about Reversible design of full adder/full subtractor in the design uses parity preserving gate used in fault tolerant systems. Normally Fredkin gate is used as parity preserving logic. The uniqueness of the system is that number of “1”s in input is equal to number of “1” s in output.

Haghparast proposed a new reversible (Binary Coded decimal) BCD subtractor using genetic algorithm in Haghparast proposed fault tolerant reversible BCD adder in the design uses fault tolerant NFT reversible gates and F2G gates. It provides an optimized design. Haghparast proposed reversible BCD adder/subtractor in the reversible BCD adder/subtractor units were designed using genetic algorithm for optimization approaches. Reversible logic is one of the most vital issue at present time and it has different areas for its application, those are low power CMOS, quantum computing, nanotechnology, cryptography, optical computing, DNA computing, digital signal processing (DSP), quantum dot cellular automata, communication, computer graphics. It is not possible to realize quantum computing without implementation of reversible logic. The main purposes of designing reversible logic are to decrease quantum cost, depth of the circuits and the number of garbage outputs. This paper provides the basic reversible logic gates, which in designing of more complex system having reversible circuits as a primitive component and which can execute more complicated operations using quantum computers. The reversible circuits form the basic building block of quantum computers as all quantum operations are reversible. This paper presents the data relating to the primitive reversible gates which are available in literature and helps researches in designing higher complex computing circuits using reversible gates.

Energy dissipation is one of the major issues in present day technology. Energy dissipation due to information loss in high technology circuits and systems constructed using irreversible hardware was demonstrated by R. Landauer in the year 1960. According to Landauer’s principle, the loss of one bit of information lost, will dissipate kT*ln (2) joules of energy where, k is the Boltzmann’s constant and k=1.38x10 -23 J/K, T is the absolute temperature in Kelvin[1]. The primitive combinational logic circuits dissipate heat energy for every bit of information that is lost during the operation. This is because according to second law of thermodynamics, information once lost cannot be recovered by any methods. In 1973, Bennett, showed that in order to avoid kTln2 joules of energy dissipation in a circuit it must be built from reversible circuits [2]. According to Moore’s law the numbers of transistors will double every 18 months. Thus energy conservative devices are the need of the day. The amount of energy dissipated in a system bears a direct relationship to the number of bits erased during computation. Reversible circuits are those circuits that do not lose information. The most prominent application of reversible logic lies in quantum computers [8].

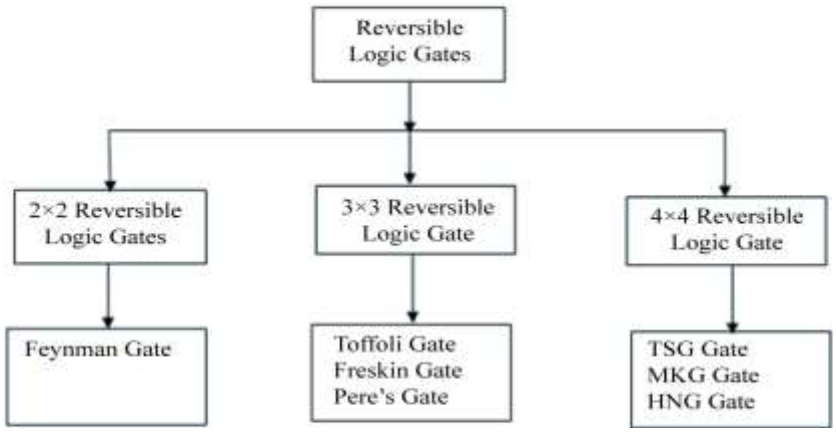

Fig 2: Classification of reversible logic gates.

A quantum computer will be viewed as a quantum network (or a family of quantum networks) composed of quantum logic gates; It has applications in various research areas such as Low Power CMOS design, quantum computing, nanotechnology and DNA computing. Quantum networks composed of quantum logic gates; each gate performing an elementary unitary operation on one, two or more two–state quantum systems called qubits. Each qubit represents an elementary unit of information; corresponding to the classical bit values 0 and 1. Any unitary operation is reversible and hence quantum networks effecting elementary arithmetic operations such as addition, multiplication and exponentiation cannot be directly deduced from their classical Boolean counterparts (classical logic gates such as AND or OR are clearly irreversible).Thus, quantum arithmetic must be built from reversible logical components [3]. Reversible computation in a system can be performed only when the system comprises of reversible gates. A circuit/gate is said to be reversible if the input vector can be uniquely recovered from the output vector and there is a one-to-one correspondence between its input and output assignments. The reversible circuits form the basic building block of quantum computers. This paper presents the primitive reversible gates which are gathered from literature and this paper helps researches/designers in designing higher complex computing circuits using reversible gates. The paper can further be extended towards the digital design development using reversible logic circuits which are helpful in quantum computing, low power CMOS, nanotechnology, cryptography, optical computing, DNA computing, digital signal processing (DSP), quantum dot cellular automata, communication, computer graphics.

CONCLUSION

Comparator designed half subtraction using TR gate shows effectiveness in terms of quantum cost but at the expense of number of reversible gates and garbage output. Reversible comparator using full subtraction algorithm proposed is performing better in terms of number of reversible gates and garbage output since equivalence checker circuit is not needed. The same algorithm may be implemented with Delay elements in between by principle of retiming to reduce critical path delay. The future scope of the work is to realize these reversible logic gates in DNA molecules and implement these arithmetic systems so as to reduce power consumption.

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