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Simulation and Analysis of 13-Levels K-Type Multilevel Inverter

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Abstract
This paper presents a new reconfiguration module for asymmetrical multilevel inverters in which the capacitors are used as the dc links to create the levels for staircase waveforms. This configuration of the multi- level converter makes a reduction in dc sources. On the other hand, it is possible to generate 13 levels with lower dc sources. The proposed module of the multilevel inverter generates 13 levels with two unequal dc sources (2VDC and 1VDC). It also involves two chargeable capacitors and 14 semiconductor switches. The capacitors are self-charging without any extra circuit. The lower number of components makes it desirable to be used in wide range of applications. The module is schematized as two back-to-back T-type inverters and some other switches around it. Also, it can be connected as a cascade modular which leads to a modular topology with more voltage levels at higher voltages. The proposed module makes the inherent creation of the negative voltage levels without any additional circuit (such as H- bridge circuit). Nearest level control switching modulation scheme is applied to achieve high-quality sinusoidal output voltage. Simulations are executed in MATLAB/Simulink and a prototype is implemented in the power electronics laboratory in which the simulation and experimental results show a good performance

Keywords: *Capacitor Voltage balancing, Asymmetric, capacitors, multilevel inverter, nearest level control switching, power electronics, self-charging.*

1. Introduction

Multilevel inverters (MLIs) have been providing the reliable and high-quality voltage source converters to connect the dc power systems to the ac power systems. MLIs with different configurations are one of the interesting devices in the power electronics area. The verity of configuration spreads them as a wide range application in power system, recently. The abilities of MLIs in medium/high power applications against two levels inverters make them leading converters in photovoltaic systems [1], HVdc for transmission line [2], [3], wind, turbine [4], active power filer [5], drives systems [6], [7], electrical vehicle [8], and power grid [9]. MLIs have high resolution on the output voltage and low harmonic components because of a high number of output levels. They also have low stress on switches, modularity, and scalability due to cascade connection ability. Multilevel converters are introduced into neutral point clamped (NPC) [10], flying capacitor (FC) [11], and cascade H-bridge (CHB) [12]. Unbalanced dc links and high stress on switches are the disadvantages of NPC and FC, also including huge capacitors. Therefore, CHB types are focused by re- searchers, and reduced numbers of components are targeted in the configuration of CHB topologies. This kind of topologies are comparable from different aspects such as the number of levels, the number of dc sources, the number of semiconductors, total standing voltage (TSV), the inherent creating of negative levels, etc.; some reviewing studies are presented in [13]–[16] for last decade topologies. A dc source generates one level by two switches in [17] and makes one module, together. The module can be connected in series to create more levels. On the other side, all levels are positive levels then it needs an additional circuit to create negative levels. H-bridge is added to the series modules in [18] for staircase sinusoidal waveform (negative and positive half-cycles). The semiconductors in H-bridge circuits, which create negative voltage levels, tolerate high switching stress. Generally, MLIs arrange different connections of semi- conductor switches to synthesize several small voltage steps to form a staircase output waveform. Using lower components to produce higher output voltage levels is one of the important issues in the configuration of MLIs. Applying unequal dc links is the best method to achieve this issue. Asymmetric multilevel inverters with unequal dc links present a new type of configuration, which reduces the number of components along with higher output voltage levels. Modules are designed based on adding or subtracting of dc links by power electronics semiconductors. On another side, the stress on switches should be considered in asymmetric multilevel inverters due to unequal dc sources. The stress on switches is introduced with TSV, which is a total highest voltage of each switch in off mood. Gupta and Jain [19], and Kangarlu and Babaei [20] introduced crossing switches for opposite polarity of dc links to generate more levels and dividing of stress on switches. Extended H-bridge with different amount of dc links is presented in [21] and [22]. Higher levels in theses topologies are along with stress on switches that need higher rate semiconductor. Hybrid-type

topologies are proposed as another type of MLIs in [23]. Samadaei et al. [24], [25] introduced modules with low semiconductors with inherent negative.

2. Circuit Configuration and its Operation

The circuit diagram of the three-phase MMC shown in Fig.1 shows a general conceptual diagram of multilevel inverters. A suitable designing of power converter can achieve maximum output levels from two dc sources. It is possible to use capacitors to create some extra dc links to get more levels than expected. In this kind of configuration, the charging path of capacitors should be provided in addition to the output levels paths. It would be interesting to not use an additional circuit for the charging of capacitors.

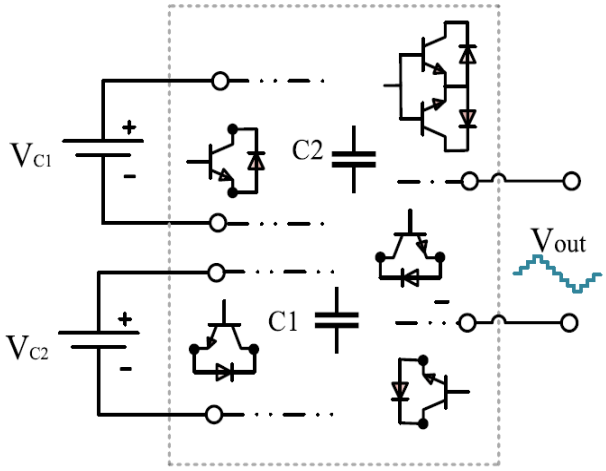


Fig. 1 Basic cell of single-phase K-type multilevel inverter

3. Circuit Model and its Working Principal

There are two dc sources with different amounts as 1VDC and 2VDC. Using unequal dc sources for asymmetric multilevel inverters product different number of output voltage levels by fewer semiconductors and lower harmonic components as well. It would be better to create two extra dc links with capacitors. In total, it gives four dc links. Fig.2 introduces the proposed module with a new component arrangement including 14 switches (8 unidirectional switches and 3 bidirectional switches), 14 diodes, and two unequal dc source, and two capacitors. This configuration generates six positive levels, six negative levels, and zero level (13 levels totally). The shape of the proposed topology is similar to Kite and it is named “K-Type” (Kite Type).

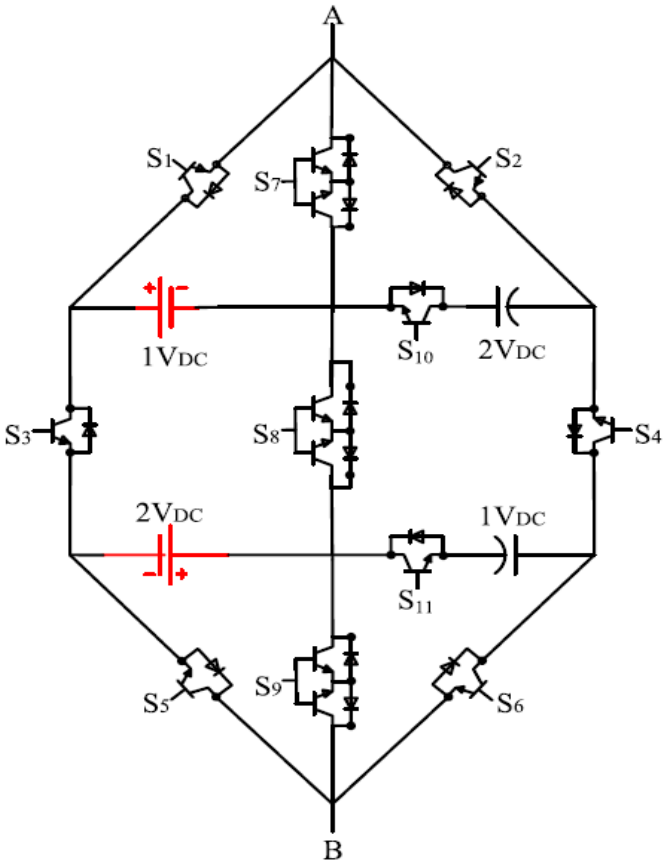


Fig. 2 Generalized single-phase K-Type MLI module

The main concept of this circuit is creating different paths from different sides of a dc link to be connected to other dc links to create negative levels in order to remove H-bridge. It is noticeable that the dc source with 1VDC charges the capacitor with 1VDC, and the dc source with 2VDC charges the capacitor with 2VDC without any additional circuit. Fig.3 and Table.1 show switching patterns of the output levels in the proposed structure. The designing of the module and their switching paths are selected smartly in such a way that there are no positive poles of dc links on the anode side of diode to conduct. In addition, Figure 3.3 depicts the switching paths does not form any close loop for dc links. Thus, diodes polarity and bidirectional switches guarantee that for suppressing of switches short-circuiting will be not occurred in the module.

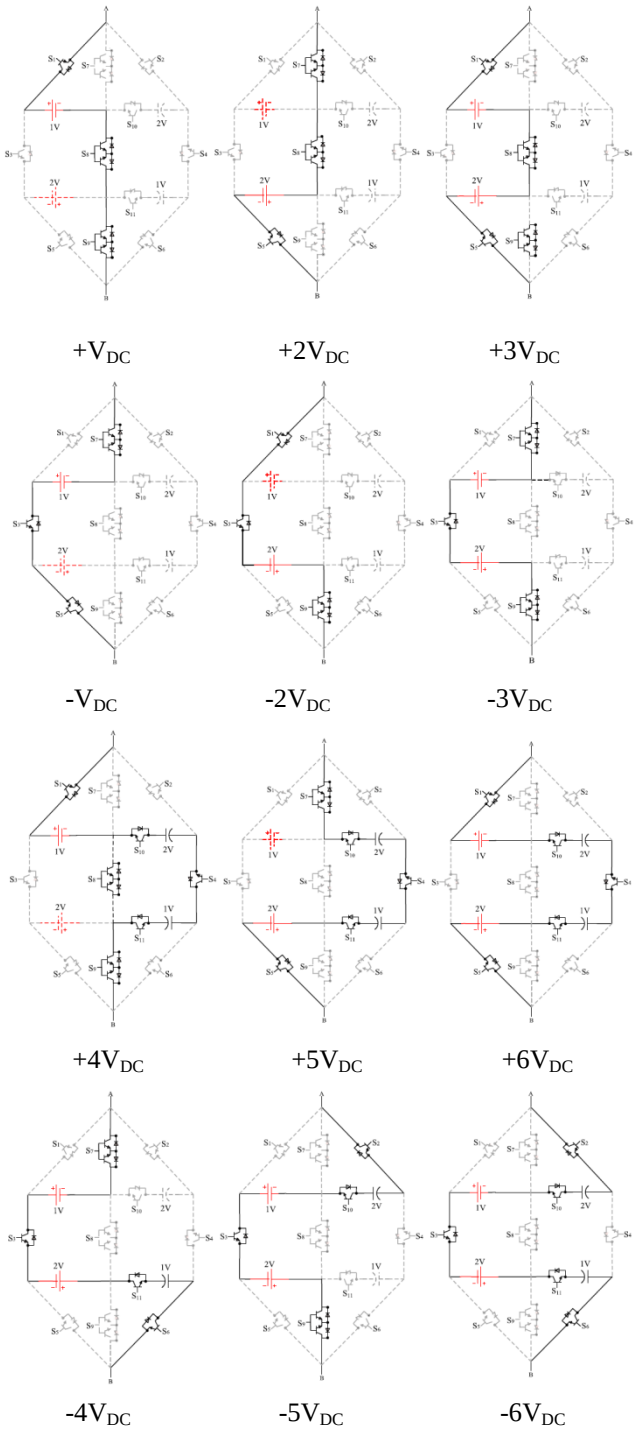


Fig. 3 Different Switching Modes

Table 3.1 indicates switch modes in each levels. Also there are redundant paths for some levels from other dc links. Switch (S_1 , S_7), (S_3 , S_8), and (S_5 , S_9) cannot be turned ON at the same time to prevent the short circuit between two dc sources. Number of switches turning on per one cycle for each switch is shown in the last row of Table 3.1. Fig. 3 shows the schematic output voltage of the proposed inverter with the associated pulse pattern in one cycle of fundamental voltage. As shown in Fig. 3, switches S_2 , S_3 , S_4 , and S_8 are turned ON in low frequency, which reduces switching losses. Other switches also operate in a reasonable switching frequency. It also shows employed dc sources and capacitors for each level. Capacitors as the dc links are used in levels 4th, 5th, and 6th. Consequently, two unequal dc sources with the proposed module create the 13-levels modulefor multilevel inverters.

Table. 1 Switching Modes of 13-level Asymmetric K-Type Configuration

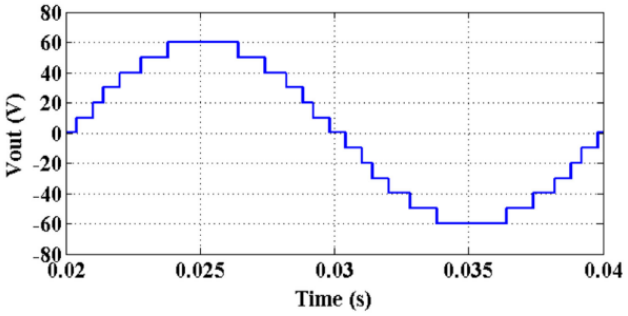
O/P	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8	S_9	S_{10}	S_{11}
$+6V_{DC}$	1	0	0	1	1	0	0	0	0	1	1
$+5V_{DC}$	0	0	0	1	1	0	1	0	0	1	1
$+4V_{DC}$	1	0	0	1	0	0	0	0	1	1	1
$+3V_{DC}$	1	0	0	0	1	0	0	1	0	0	0
$+2V_{DC}$	0	0	0	0	1	0	1	1	0	0	0
$+V_{DC}$	1	0	0	0	0	0	0	1	1	0	0
$-V_{DC}$	0	0	1	0	1	0	1	0	0	0	0
$-2V_{DC}$	1	0	1	0	0	0	0	0	1	0	0
$-3V_{DC}$	0	0	1	0	0	0	1	0	1	0	0
$-4V_{DC}$	0	0	1	0	0	1	1	0	0	0	1
$-5V_{DC}$	0	1	1	0	0	0	0	0	1	1	0
$-6V_{DC}$	0	1	1	0	0	1	0	0	0	1	1

4. Simulation Results

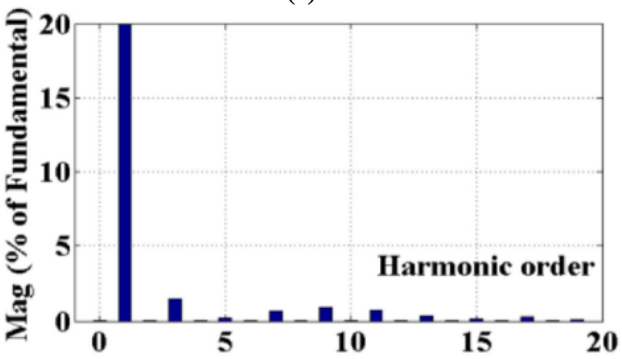
The proposed multilevel inverter is simulated by MATLAB/SIMULINK to examine the performance of the proposed module. The simulation parameters are illustrated in Table 2. Fig. 4 (a) shows the output voltage of 13-levels for the proposed multilevel inverter with switching technique NLC. Each level (V_{DC}) is 10 V to create 50 Hz sinusoidal waveform. Fig.4(b) also illustrates harmonics spectrums that validate each harmonic order is in low range. THD% is calculated as 3.87% by FFT analysis for waveform of Fig.4(a), which satisfied IEEE519 (THD% ≤ 8% and each order ≤5%). The proposed K-type topology load current waveform in an asymmetric configuration is shown in Fig.5. Fig. 6 illustrates the voltage across capacitors (C_{L1} *and* C_{L2}) in an asymmetric configuration. Similarly, Fig. 7 shows the voltage across capacitors (C_{R1} *and* C_{R2}) in an asymmetric configuration.

Table 4.1 Simulation Parameters

Parameters	Ratings
Rated DC voltage	$V_{DC1} = 12V$ & $V_{DC2} = 24V$
Capacitors	$C_1 = C_2 = 2200\mu F$
Modulation index	m_a = 0.85
Load value	R=20 Ω, L= 20 mH
Modulating wave frequency	f_m =50 Hz
Switching frequency	f_s =3150 kHz



(a)



(b)

Fig. 4 Output voltage of proposed K-type topology

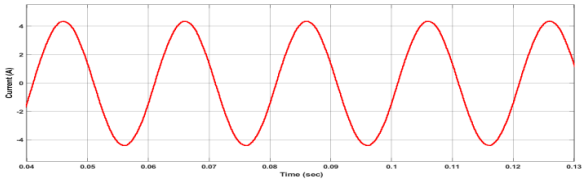


Fig. 5 Load current of proposed K-type topology

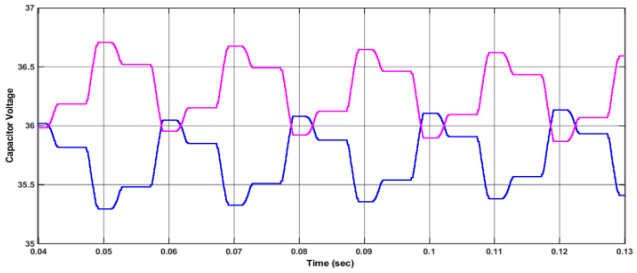


Fig. 6 Voltage across capacitors (C_{L1} and C_{L2})

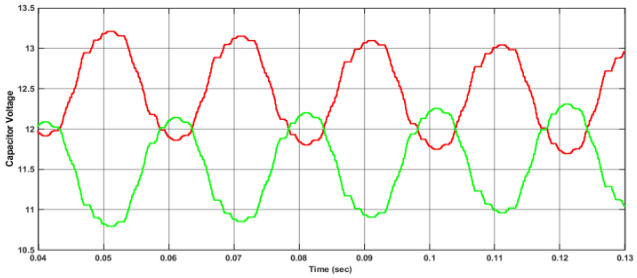


Fig. 7 Voltage across capacitors (C_{r1} and C_{r2})

5. Conclusion

This paper introduced one module for asymmetrical multilevel inverter to produce 13 levels by two dc sources. The proposed multilevel is designed based on two back-to-back T-Type modules with some switches around them. The proposed module is named K-Type. The configuration of K-type provides two extra dc links by capacitors (as the virtual dc supply) to achieve more levels to create staircase waveform. The module needs lower components including 2 dc sources, 2 capacitors, and 14 semiconductors. It can be used in power applications with unequal dc sources (with ratio 1:2). It can also be easily modularized in two strategies in cascade arrangements to form high-voltage outputs with low stress on semiconductors and lowering the number of devices. This ability can be used in some special applications such as solar farm along with a lot of dc sources. DC sources can also have different voltage amplitudes. In the conventional methods, one inverter for each dc resources should be considered and fix the output voltage with the same amplitude. It increases the complexity and losses from this aspect, but in asymmetrical multilevel converters, it is possible to combine some dc resources together and generate a unique ac output. It reduces the number of separated inverter, components, losses, etc.

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